REMARKS

The present application was filed on February 11, 2004 with claims 1-22. In the outstanding Office Action dated March 22, 2005, the Examiner has: (i) objected to the drawings; (ii) rejected claim 1 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 3,760,272 to Battes (hereinafter "Battes"); (iii) rejected claims 1-7, 15 and 16 under §102(b) as being anticipated by U.S. Patent No. 4,071,822 to Kamiya (hereinafter "Kamiya"); (iv) rejected claim 8 under 35 U.S.C. §103(a) as being unpatentable over Kamiya, in view of U.S. Patent No. 5,859,461 to Bonaccio et al. (hereinafter "Bonaccio"); (v) rejected claims 9-11 and 17-19 under §103(a) as being unpatentable over Kamiya, in view of Battes; and (vi) indicated that claims 12-14 and 20-22 are allowable.

In this response, claims 1-7, 9, 10, 12, 15-18 and 20 have been amended. An acknowledgment of the receipt of formal drawings filed on March 29, 2004 is hereby requested. Applicants traverse the objection to the drawings, as well as the §102(b) and §103(a) rejections, for at least the reasons set forth below. Applicants respectfully request reconsideration of the present application in view of the above amendments and the following remarks.

The Examiner has objected to the drawings for failing to show every feature of the invention specified in the claims. Specifically, the Examiner contends that FIG. 2 fails to show the feature "a passive load connected between the third terminal of the at least one transistor and a second voltage supply," as recited in claims 1 and 15. The Examiner states that, "Fig. 2 shows, a passive load 204 connected between third terminal D of transistor MP1 and ground. Therefore the second supply voltage appears to be missing in this figure" (Office Action; page 2, paragraph 1). Applicants respectfully disagree with this contention.

First, as set forth in 35 U.S.C. §113, a drawing need only be furnished "where necessary for the understanding of the subject matter sought to be patented." Applicants submit that the present specification provides a clear and unambiguous description for this feature of the claimed invention, and thus it is believed that such feature need not be explicitly depicted in the drawing. Nevertheless, Applicants submit that the passive load connected between the third terminal of the at least one transistor and a second voltage supply is clearly shown in FIG. 2, for the exemplary case where the second supply voltage is ground, and in FIG. 4, for the exemplary case where the second supply voltage is VDD. The specification states that resistor 204, "or a suitable alternative passive load,"

is connected between node N1 (the third terminal of the transistor) and "a negative voltage supply of the circuit, which may be ground" (Specification; page 5, lines 18-20, emphasis added). Consequently, since the second voltage supply is depicted in FIG. 2 for the illustrative case in which the second voltage supply is ground, Applicants do not believe that any modification of the drawings is required.

For at least the above reasons, Applicants submit that all elements recited in the claims that are necessary for a proper understanding of the invention are clearly depicted in the drawings. Accordingly, withdrawal of the objections to the drawings is respectfully solicited.

Claims 12 and 20, which the Examiner has indicated as being allowable, have been rewritten in independent form including all of the limitations of the respective base claims and any intervening claims. Accordingly, favorable allowance of claims 12 and 20, and the respective claims depending therefrom, is respectfully requested.

Claim 1 stands rejected under §102(b) as being anticipated by Battes. The Examiner contends that Battes discloses all of the elements set forth in the subject claims. Applicants respectfully disagree with this contention. Battes is directed to a high impedance signal level detector wherein "pairs of electronic pulses may be generated in which the elapsed time between the pulses in each pair is as directly proportional as desired, or nearly so, to the amplitude of an applied DC voltage" (Battes; Abstract). The circuit disclosed in Battes, however, is not capable of functioning where there is a mismatch between a battery voltage and the positive supply voltage of the detector circuit, and thus does not solve an important problem to which the claimed invention is directed (*see, e.g.*, Specification; page 4, beginning at line 16).

Claim 1 is distinguishable from Battes. For example, Battes fails to disclose a passive load connected between the third terminal of the transistor and a second voltage supply, as required by claim 1. The potentiometer (17), which the Examiner analogizes to the passive load recited in claim 1, is connected between the collector terminals of transistors 5 and 6, with a wiper terminal of the potentiometer being connected to ground. This connection arrangement, however, is not analogous to the configuration recited in claim 1 of the present application. Battes also fails to disclose a detector circuit which is configured to generate an output signal being a first value indicating that the input signal is substantially at a first voltage level and being a second value indicating that the

input signal is substantially at a second voltage level, as required by claim 1. Rather, the circuit disclosed in Battes is configured to generate pairs of output pulses "in which the elapsed time between the pulses in each pair is as directly proportional as desired, or nearly so, to the amplitude of an applied D.C. voltage" (Battes; column 4, lines 39-43; emphasis added). Thus, in the circuit taught by Battes, it is not the voltage level of the output signal which is indicative of the DC level of the input signal, rather it is the elapsed time between pulses which is indicative of the DC level of the input signal. This is clearly distinguishable from the invention set forth in claim 1.

Notwithstanding the above traversal, independent claim 1 has been amended to further define the invention. Claim 1, as amended, further defines the detection circuit as being configurable for comparing a first voltage supply with at least a second voltage supply and for indicating a voltage level of the second voltage supply, the detection circuit including:

> at least one transistor, the at least one transistor including a first bias terminal connecting to the first voltage supply, a control terminal for receiving the second voltage supply, and a second bias terminal operatively coupled to an output of the circuit; and
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> a passive load connected between the second bias terminal of the at least one transistor and a third voltage supply;
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> wherein the detection circuit is configured to generate an output signal at the output of the circuit, the output signal being at a first logic value indicating that the second voltage supply is substantially at a first voltage level, and the output signal being at a second logic value indicating that the second voltage supply is substantially at a second voltage level, the first and second voltage levels defining an operating voltage range of the second voltage supply;
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> wherein when the second voltage supply is at one of the first and second levels, the detection circuit draws substantially no current.

The prior art of record fails to teach or suggest at least these features of amended claim 1.

For at least the above reasons, Applicants assert that claim 1 is patentable over the prior art. Accordingly, favorable reconsideration and allowance of claim 1 are respectfully solicited.

Claims 1-7, 15 and 16 stand rejected under §102(b) as being anticipated by Kamiya. With regard to independent claims 1 and 15, which are of similar scope, the Examiner contends that Kamiya discloses all of the features set forth in these claims. Applicants respectfully disagree with this contention. Kamiya is directed to a voltage detecting circuit operative to convert the voltage

of the power source into a time value, and to display this time value digitally (Kamiya; column 1, lines 26-31).

Claims 1 and 15 are distinguishable from Kamiya. For instance, Kamiya fails to disclose a passive load connected between the third terminal of the transistor and a second voltage supply. Resistor 14, which the Examiner analogizes to the passive load recited in claims 1 and 15, is not connected between the third terminal of the transistor and a second voltage supply, but is instead connected between the drain of transistor 6 and the drain of a second transistor 7, which is not analogous to a second voltage supply. Kamiya also fails to disclose a detector circuit which generates an output signal being a first value indicating that the input signal is substantially at a first voltage level and being a second value indicating that the input signal is substantially at a second voltage level. Rather, the circuit disclosed in Kamiya is configured to generate "an output signal having a time width corresponding to the drop of the power source voltage so that the drop of the power source voltage can be displayed digitally" (Kamiya; column 6, lines 27-30). Since the output voltage of a power source is converted to a time signal by the circuit taught in Kamiya (Kamiya; Abstract), the voltage level of the output signal in Kamiya is not indicative of the DC level of an input signal applied to the circuit, as required by the subject claims.

Notwithstanding the above traversal, claims 1 and 15 have been amended to further define the invention, as described above. The cited prior art fails to teach or suggest at least these features of amended claims 1 and 15.

For at least the above reasons, Applicants assert that claims 1 and 15 are patentable over the prior art. Accordingly, favorable reconsideration and allowance of claims 1 and 15 are respectfully requested.

With regard to claims 2-7, which depend from claim 1, and claim 16, which depends from claim 15, Applicants submit that these claims are also patentable over the prior art of record by virtue of their dependency from their respective base claims, which are believed to be patentable for at least the reasons set forth above. Moreover, one or more of these claims define additional patentable subject matter in their own right. For example, claim 7 further defines the at least one transistor in the circuit as comprising an NMOS device. The prior art of record does not disclose at least this additional feature of the subject claims.

For at least the reasons set forth above, claims 2-7 and 16 are believed to be patentable over the prior art, not merely by virtue of their dependency from their respective base claims, but also in their own right. Accordingly, favorable reconsideration and allowance of claims 2-7 and 16 are respectfully requested.

Claims 8-11 and 17-19 stand rejected under §103(a) as being unpatentable over Kamiya, in view of either Bonaccio or Battes. The Examiner contends that the combination of either Kamiya and Bonaccio or Kamiya and Battes teaches or suggests all of the features set forth in the subject claims so as to render the subject claims unpatentable. Applicants respectfully disagree with this contention and assert that claims 8-11, which depend from claim 1, and claims 17-19, which depend from claim 15, are patentable over the prior art of record by virtue of their dependency from their respective base claims, which are believed to be patentable for at least the reasons given above. Moreover, one or more of these claims define additional patentable subject matter in their own right. For example, claims 9 and 17 further define the circuit as including a "voltage level shift circuit connected between the first voltage supply and the first terminal of the at least one transistor." The prior art of record does not disclose at least this additional feature of the subject claims.

With regard to claims 9 and 17, the Examiner acknowledges that Kamiya does not disclose a voltage level shift circuit (Office Action; page 6, paragraph 6). However, the Examiner contends that such a feature is disclosed in Battes as potentiometer 17. Applicants respectfully disagree with this contention. Besides already analogizing the potentiometer 17 with the passive load recited in independent claims 1 and 15, Applicants submit that potentiometer 17 disclosed in Battes does not perform a voltage level shift function. Rather, potentiometer 17 in Battes "is designed to provide for the placement of unequal loads on the outputs of amplifier transistors 5 and 6, thus allowing for precise compensation of effects due to uneven offset voltages and current gains in the various transistors" (Battes; column 2, lines 47-51). Furthermore, even assuming, *arguendo*, that the potentiometer 17 in Battes can be analogized to the voltage level shift circuit recited in the subject claims, the potentiometer is not connected between the first voltage supply and the first terminal of the at least one transistor, as required by the subject claims. Rather, the potentiometer is connected between the collectors of transistors 5 and 6, which form outputs of the detector circuit at terminals 12 and 13 (Battes; FIGURE).

Claim 10, as amended, further defines the detection circuit as comprising a voltage level shift circuit configured such that the voltage generated by the voltage level shift circuit is "greater than or equal to a difference between a maximum tolerance limit of the first voltage supply and a minimum tolerance limit of a highest expected voltage level of the second voltage supply." The prior art, when consider in combination, fails to teach or suggest at least these additional features. With regard to claim 10, the Examiner acknowledges that Kamiya does not expressly disclose a voltage level shift circuit (Office Action; page 6, paragraph 6), but does not address with specificity where in Battes such features of claim 10 are taught. While Battes discloses a potentiometer (17), the potentiometer functions to compensate for offsets between the base-emitter voltages of transistors 4 and 7, and does not provide a voltage drop between the first voltage supply and the first bias terminal of the at least one transistor that is substantially equal to "a difference between a maximum tolerance limit of the first voltage supply and a minimum tolerance limit of a highest expected voltage level of the second voltage supply," as required by claim 10.

For at least the reasons set forth above, claims 8-11 and 17-19 are believed to be patentable over the prior art, not merely by virtue of their dependency from their respective base claims, but also in their own right. Accordingly, favorable reconsideration and allowance of claims 8-11 and 17-19 are respectfully solicited.

In view of the foregoing, Applicants believe that pending claims 1-22 are in condition for allowance, and respectfully request withdrawal of the §102 and §103 rejections.

Respectfully submitted,

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